HW

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,558	06/21/2001	Jain Raj Kumar	GR 00 P 12518	7289

24131 7590 01/04/2005

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
MOAZZAMI, NASSER G	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,558	KUMAR, JAIN RAJ	
	Examiner	Art Unit	
	Nasser G Moazzami	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,15-20 and 22* is/are rejected.

7)☒ Claim(s) *9,11-14 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 15 and 16 are objected to under 37 CFR 1.75 as being a substantial duplicate each other. When two claims in an application are duplicates or else are so close in content that they both cover the same thing,despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Examiner suggests the title to be changed to "COMPUTER SYSTEM CONTAINING A PLURALITY OF CENTRAL PROCESSING UNITS HAVING A SINGLE ADDRESS BUS".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 10, 15-20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Yabushita et al. (US Patent No. 5214775), hereinafter Yabushita.

As per claims 1 and 22, Yabushita discloses a CPU system, comprising: a plurality of CPUs **[multiprocessors system (see Fig. 1]**; a common memory provided for said plurality of CPUs **[shared memory 3 (see Fig. 1)]**; an address bus for addressing said common memory **[bus from the arbiter and selector 4 to shared memory 3 (see Fig. 1)]**; at least one of said CPUs being connected to said address bus **[MPUa (see Fig. 1)]**; and other ones of said CPUs accessing said common memory via said at least one of said CPUs connected to said address bus **[MPUb accessing the shared memory 3a through the bus arbiter and selector 4a (see Fig. 1)]**.

As per claims 2-3 and 20, Yabushita discloses a data bus connected to at least one of said CPUs; and said common memory outputting, via said data bus, data read from or written to said common memory **[data line 9a is connected to the bus arbiter and selector 4a so that it is inputted to and outputted from the shared memory 3a (column 5, lines 29-35)]**.

As per claims 4 and 10, Yabushita teaches a data read bus connected to said common memory for outputting data read from said common memory; a data write bus connected said common memory for supplying data to be written into said common memory **[data line 9a is connected to the bus arbiter and selector 4a so that it is**

inputted to and outputted from the shared memory 3a (column 5, lines 29-35)]; said plurality of CPUs including a given subset of CPUs not connected to said address bus; and at least some CPUs of said given subset of CPUs being connected to at least one bus selected from the group consisting of said data read bus and said data write bus **[see Fig. 1-3]**.

As per claims 5-8, Yabushita teaches a switching apparatus which a multiplexer operatively connected to said common memory; an address memory device operatively connected to said switching apparatus; and said switching apparatus selectively supplying data output to said address bus by said at least one of said CPUs connected to said address bus and data stored in said address memory device to said common memory as an address **[arbiter and selector 4a (see Fig. 1)]**.

As per claims 15-17, Yabushita discloses that when one of said other ones of said CPUs not connected to said address bus transmits data indicating to a relevant one of said plurality of CPUs a start address for an operation selected from the group consisting of reading data from said common memory and writing data to said common memory, when one of said plurality of CPUs, which is to be used for an access and is connected to said address bus, accesses said common memory **[when MPUb is trying to access the shared memory 3a either for reading or writing to the shared memory, it will provide the address for the operation to be carried out (see column 5, line 53 through column 6, line 68; also see Fig. 2-3)]**; a switching

apparatus operatively connected to said common memory; an address memory device operatively connected to said switching apparatus; driving said switching apparatus such that data stored in said address memory device are supplied to said common memory as an address; notifying a specific one of said plurality of CPUs, which requested access to said common memory, that said specific one of said plurality of CPUs is allowed to perform an operation **[arbiter and selector 4a (see Fig. 1); in accordance with the arbitration results, selecting a processor (column 8, lines 28-57)]**.

As per claims 18-19, Yabushita teaches that the other ones of said CPUs output signals, the signals representing addresses and being converted and used as control signals for controlling system components **[decoding and translating the address]**.

Allowable Subject Matter

5. Claims 9, 11-14 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nasser G Moazzami whose telephone number is (571) 272-4195. The examiner can normally be reached on 7:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NASSER MOAZZAMI
PRIMARY EXAMINER

12/21/2004